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***Abstract*—A receiver composed by a graphene FET 200-GHz mixer and a 1-GHz intermediate frequency amplifier integrated on a silicon substrate was modelled, fabricated and characterized. This is the first demonstration of a millimeter wave integrated receiver based on graphene FETs. The receiver conversion loss is measured to be 25 dB across the 185-205-GHz band with 16 dBm of local oscillator pump power, which is in good agreement with the circuit simulations. The simulations show that the receiver conversion loss can be significantly reduced to 16 dB by reducing the contact resistance and by realizing a higher charge carrier mobility in the mixer transistor.**

I. INTRODUCTION

As high-speed communication systems are evolving, the need for new materials and technologies arises, which allow for the development of advanced millimeter wave and terahertz circuitry [1, 2]. In this context, a receiver is an important system component. A typical heterodyne receiver consists of an antenna, filters, amplifiers, and a down converting mixer. Usually, the amplifiers and the mixers are based on field-effect transistors (FETs) [3]. To realize high speed amplifier FETs the charge carrier mobility and velocity in the transistor channel should be high. In this context, the 2D material graphene is a promising candidate, since it reveals high room temperature charge carrier mobility and saturation velocity [4]. Graphene FETs (GFETs) with a current and power gain comparable to that of Si n-channel MOSFETs have been demonstrated [5]. Still, the power gain of GFETs lays behind that of InP and GaAs transistors, partly, due to the lack of a bandgap in graphene. However, the application of GFETs in subharmonic resistive mixers utilizes the unique symmetric resistance characteristics of GFETs (attributed to the lack of the bandgap) allowing a simplified receiver circuitry, since no balun is required. The simplification of the circuitry and the potential of graphene being grown in large scale and being transferred to any arbitrary substrate, explains the interest of developing a receiver circuit fully based on GFETs. In our recent works a 10-dB small-signal amplifier designed for 1 GHz and a 200 GHz subharmonic resistive mixer based on graphene FETs (GFETs) have been demonstrated [6, 7]. In this work the GFET-mixer and IF amplifier are integrated together on a silicon substrate chip, as shown in Fig. 1 and the characterization results are presented.

II. METHODS

The integrated receiver is implemented in CPW technology and designed using equivalent circuit, full-wave EM, and harmonic balance simulations. The equivalent circuit simulations are used to simulate and optimize the dc and rf performances of the GFETs, the full-wave EM simulations are performed to simulate and optimise the coplanar waveguide circuitry, the planar spiral inductor, as well as a metal-insulator-metal (MIM) capacitor, and the harmonic balance simulations are carried out to simulate the full receiver performance. The mixer layout is as that reported in [7]. The mixer GFET channel is designed as an array of bow-tie-shaped nano-constrictions with the aim to increase the on-off ratio, hence, the mixer gain, and to provide impedance matching. The effective channel width due to the nano-constrictions is $W_{channel}$ = 2x6 μm, whereas the deigned gate width is W_{gate} = 2x40 μm. The bandstop and bandpass filters are designed as quarter wavelength open stub and coupled CPW lines. Metal airbridges in the CPW lines are included to suppress the parasitic slotline modes. The IF amplifier prototype, presented in [6], is further developed by optimizing the gate width and length dimensions, W and L_g, for maximal gain using a large-signal equivalent circuit model as in [8] and shown in Fig.2, with the modification of including parasitic resistances, R_{pg} and R_{pd}, in parallel to the parasitic pad capacitances C_{pg} and C_{pd}. The optimisation resulted in W = 2x120 µm and L_g = 1 µm. Additionally, the lumped inductor of the input impedance matching circuitry is replaced by a planar inductor to be fully MMIC compatible.

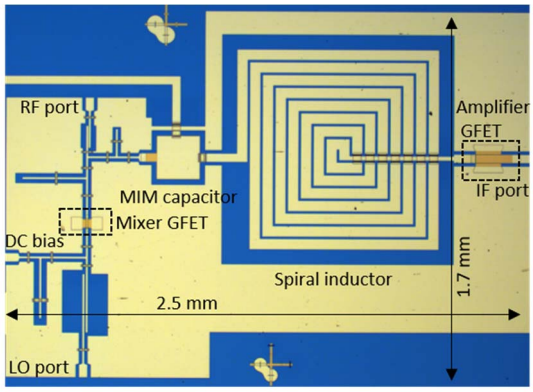

Fig. 1. Micrograph of the receiver composed by integrated GFET mixer and IF amplifier with CPW filters, MIM capacitor and spiral inductor of the impedance matching circuitry.

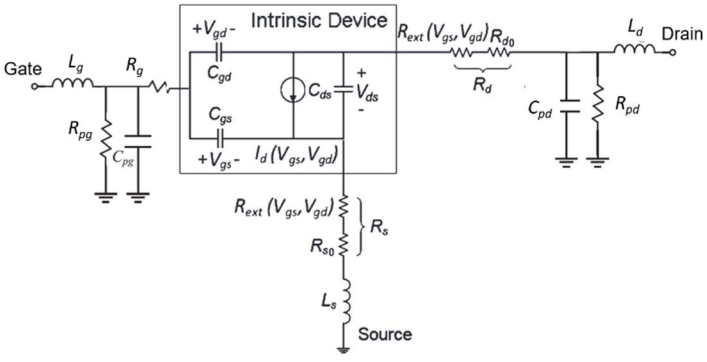

Fig. 2. Large signal equivalent circuit of a GFET [8] modified with parasitic resistances, R_{pg} and R_{pd}, in parallel to the parasitic pad capacitances C_{pg} and C_{pd}.

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	C_{gd} (fF)	C_{gs} (fF)	C_{ds} (fF)	C_{pg} (fF)
Mix	6	7	17	5
Amp	200	500	5	5
	C_{pd} (fF)	L_g (pH)	L_s (pH)	L_d (pH)
Mix	5	50	6	20
Amp	5	50	5	30
	R_{pg}/R_{pd} (Ω)	R_i (Ω)	R_0 (Ω)	R_{ext} (Ω)
Mix	8000	50	40	9
Amp	8000	5	7	1.7
	α (s/F)	V_0 (V)	μ (cm^2/Vs)	n_0 x 10^{16} (m^{-2})
Mix	344	0.5	600	1.2
Amp	20	0.37	1300	1

TABLE I. MODEL PARAMETERS OF THE LARGE-SIGNAL EQUIVALENT CIRCUITS FOR THE MIXER AND AMPLIFIER GFETS.

Airbridges are overlapping the CPW line to form the loops of the inductor. For dc isolation between the amplifier and the mixer the MIM capacitor with 200 µm^2 area and a 30 nm Al_2O_3 dielectric layer is included at the mixer IF output as shown in Fig. 1. The dc isolation allows for different bias conditions of the mixer and amplifier GFET. The spiral inductor and MIM capacitor were simulated in EM simulations and then modelled as lumped elements in the harmonic balance simulator, e.g. as an inductor (L_{in} = 20 nH) in series with a resistor (R_{in} = 30 Ω) between two shunt capacitors ($C_{in,p}$ = 216 fF) and a pi-capacitor ($C_{cap,s}$ = 82 pF, $C_{cap,p}$ = 10 fF), respectively. The values of the lumped elements are found by fitting the S-parameters simulated in the EM simulations. For the mixer GFET and the amplifier GFET the values of the large-signal equivalent circuit elements shown in Fig. 2, e.g. the parasitic and intrinsic capacitances and resistances, are obtained from S-parameters of separate mixer and amplifier measurements following the commonly used parameter extraction methods [8, 9, 10]. The GFET specific parameters, such as the mobility, contact resistance and residual charge carrier concentration, are extracted from fitting a resistance model to measured transfer characteristics of the mixer and amplifier GFET [9]. The values of the model parameters are summarised in Table I. The transfer characteristics of the mixer of this work and the mixer in [7] are shown in Fig. 3. The extracted mobility and contact resistance, of the mixer GFET used in this work in comparison with the

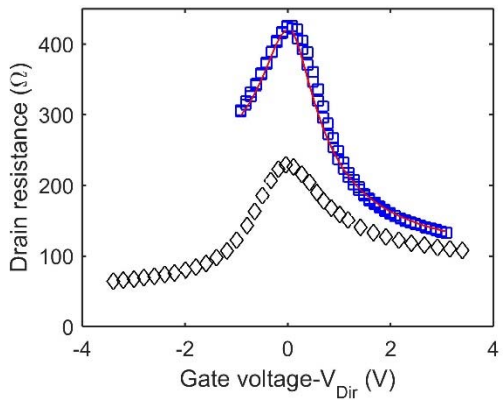

Fig.3. Measured (blue squares) and simulated (red solid line) transfer characteristic of the mixer GFET together with the measured transfer characteristic of the mixer GFET in [7] (black diamonds).

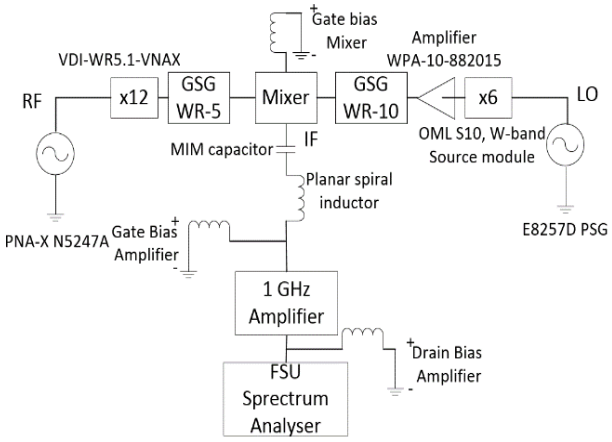

Fig. 4. Schematic block diagram of the measurement setup.

values published in [7] are R_0 = 40**Ω**, μ_e=600 cm^2/Vs and R_0 = 18**Ω**, μ_e=1100 cm^2/Vs, respectively. The on-off ratio ≥4 is similar, although the overall resistance of the mixer GFET in this work is larger. Variations of the performance between different GFETs are commonly observed.

A block diagram of the receiver measurement setup is shown in Fig. 4. The mixer is fed with a -4 dBm RF signal to the GFET drain and a 16 dBm LO signal to the gate; the frequencies are swept within 180-220 GHz and 90.5-110.5 GHz, respectively. The output powers on the RF and LO ports are measured with an Erickson power meter at the waveguide output of the VDI-WR5.1 extender and the WPA-10-882015 amplifier. The RF power and LO power are larger than those used in [7] (RF power = -10 dBm and LO power = 10 dBm) since the PNA is not used for power leveling at the RF port and another amplifier is used in the LO chain. The losses in the corresponding probes are subtracted. The optimal dc bias for the mixer and the amplifier are found by minimizing the measured conversion loss (CL).

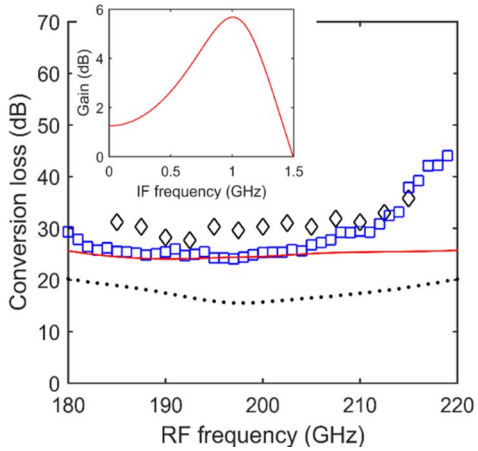

Fig.5. Measured (blue squares) and simulated (red solid line) conversion loss (CL) of the integrated receiver in this work. The measured CL of the mixer in [7] (black diamonds) and the simulated CL for an integrated circuit with IF amplifier and 16 dBm LO power assuming a mixer GFET with the same performance (black dotted line). The inset shows the simulated IF amplifier gain.

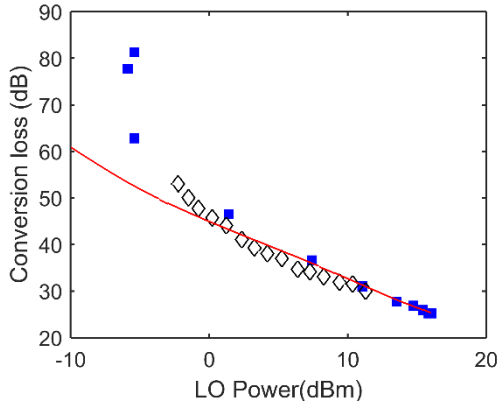

Fig.6. Measured (blue squares) and simulated (red solid line) conversion loss of the integrated receiver versus LO power compared to the mixer in [7] (black diamonds.).

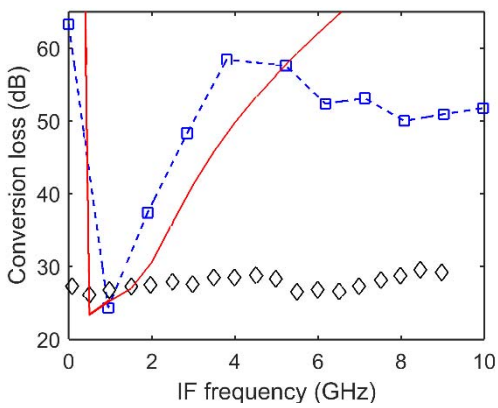

Fig.7. Measured (blue squares) and simulated (red solid line) conversion loss of the integrated receiver versus IF frequency compared to the mixer in [7] (black diamonds.).

III. Results

Fig. 5 shows the measured CL of the receiver versus RF frequency. The CL is 25 dB at the design frequency of 200 GHz. This is a 4-dB improvement compared to CL = 29 dB measured in [7]. The red solid line in Fig. 5 represent the results of the harmonic balance simulation for the integrated receiver. The simulated CL agrees reasonably well with the measurements. The increase of CL above 210 GHz can be explained by a drop of the inserted LO power from 16 dBm to 8 dBm, which was observed during the power calibration. The modelled amplifier gain is ~5 dB (inset in Fig. 5), which is in good agreement with separate amplifier measurements. The amplifier gain is limited mainly by resistive losses in the inductor. The gain can be increased up to ~10 dB if the metal thickness of the spiral inductor is increased up to 2 µm. Despite using GFET amplifier, the conversion loss versus LO power for the receiver in this work is not superior to only the mixer in [7], as can be seen in Fig. 6. The improvement of CL from 29 dBm down to 25 dBm can be attributed to higher applied LO power (16 dBm instead of 10 dBm). The expected receiver performance improvement is limited by the 4 times larger resistance of the mixer GFET used in this work (see Fig. 3). Assuming a mixer GFET performance as in [7], -4 dBm RF and 16 dBm LO power, as in this work, the minimum simulated CL is ~16 dB, as shown by the black dotted line in Fig. 5. The simulations show, that optimizing the resistance and, thereby the impedance level, strongly affects the CL. Fig. 7 shows the IF bandwidth of the receiver compared to the mixer in [7]. The IF bandwidth is strongly reduced since the amplifier is optimized for an IF frequency of 1 GHz. This behaviour is well reflected by the simulations in the IF frequency range of 0 to 4 GHz.

In conclusion, the presented work is the first demonstration of a millimetre wave GFET receiver, composed by a 200 GHz mixer and 1GHz IF amplifier integrated on a Si substrate. The receiver exhibits a CL down to 25 dB. For comparison, the lowest CL reported for a GFET based mixer is 14 dB, however, operating at a much lower RF frequency (f_{RF} = 2 GHz) [11]. Compared to implementations in other technologies, e.g. GaAs mHEMTs, with CLs of 11.4 dB [12] the CL of the demonstrated GFET receiver is still higher. However, the simulations show, that development and optimization of the GFETs and passive components will allow for further improvement of the receiver performance. In future work the performance of the GFETs will be enhanced by reducing the contact resistance and increasing the mobility/saturation velocity by modifying the fabrication process. Potentially, the gate length of the amplifier GFET can be scaled down enabling the application at RF frequencies. This allows to extend the receiver circuitry with a RF amplifier at the RF port, which is compatible with the fabrication process, to further minimise the CL.

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References

[1]. J. Wells, “Faster than fiber: The future of multi-G/s wireless,” IEEE Microw. Mag., vol. 10, n0.3, pp. 104-112, May 2009.
[2]. D.S. Green. C.L. Dohrman, J. Demmin, Y. Zheng, and T.-H. Chang. “A Revolution on the Horizon from DARPA: Heterogeneous Integration for Revolutionary Microwave\/Millimeter-Wave Circuits at DARPA: Progress and Future Directions.” IEEE Microw. Mag., vol.18, pp. 44-59, 2017.
[3]. J.B. Hagen, “Radio-Frequency Electronics: Circuit and Applications,” Cornell University, New York, 2009.
[4]. F. Schwierz, “Graphene Transistors: Status, Prospects, and Problems,” IEEE, vol. 101, Jul. 2013.
[5] . H. Lyu *et al*., “Deep-submicron Graphene Field-Effect Transistors with state-of -Art f_{max},” Scientific Reports, vol. 6, 35717, Oct. 2016.
[6]. M. Andersson, O. Habibpour, J. Vukusic, and J. Stake, “10 dB small-signal graphene FET amplifier,” Electronic Letters, vol. 48, no. 14, Jul. 2012.
[7]. M. Andersson, Y. Zhang, and J. Stake, “A 185-215-GHz Subharmonic Resistive Graphene FET Integrated Mixer on Silicon,” IEEE Trans. Microw. Theory, vol. 65, no. 1, pp. 165–172, Jan. 2017.
[8]. O. Habibpour, J. Vukusic, and J. Stake,”A Large-Signal Graphene FET Model ,” IEEE Trans. Electronic Dev., vol. 59, no. 4, pp. 968-975, Apr. 2012.
[9]. G. Dambrine, A. Cappy, F. Helidore, and E. Playez, “A new method for determining the FET small-signal equivalent circuit,” IEEE Trans. Microw. Theory, vol. 36, no. 7, pp. 1151-1159, Jul. 1988.
[10]. R. Tayrani, J. E. Gerber, T. Daniel, R. S. Pengelly, and U. L. Rohde, “A new and reliable direct parasitic extraction method for MESFETs and HEMTs,” Microwave Conference, 1993. 23rd European, pp. 451-453, Sep. 1993.
[11]. J. S. Moon, *et al.,* “Graphene FETs for Zero-Bias Linear Resistive FET Mixers,” IEEE Electronic Device Lett., vol. 34, no. 3, pp. 465-467, Mar. 2013.
[12]. I. Kallfass *et al*., "MMIC chipset for 300 GHz indoor wireless communication," Microwaves Communications Antennas and Electronic Systems (COMCAS) 2015 IEEE International Conference on, pp. 1-4, 2015.